



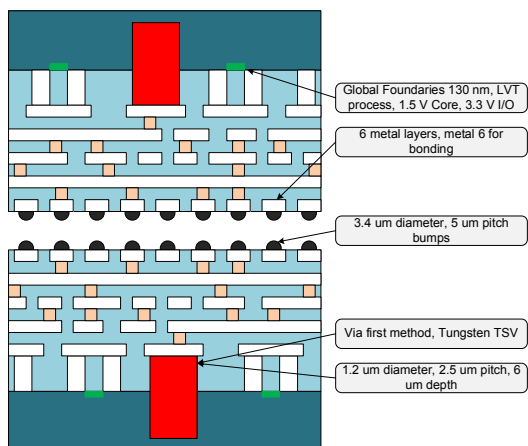
## Motivations

- state of the art of 3D implementation [2] [3] [4] [5] [6] does not consider complete multiprocessor with NoC architecture
- how much performance improvement (speedup, execution cycles) of parallel application in 3D architecture

## Objectives

- to demonstrate complete multiprocessor with 3D NoC architecture
- to propose a design methodology for exploring multiprocessor design in 3D
- to evaluate performance improvement of parallel applications in 3D NoC architecture

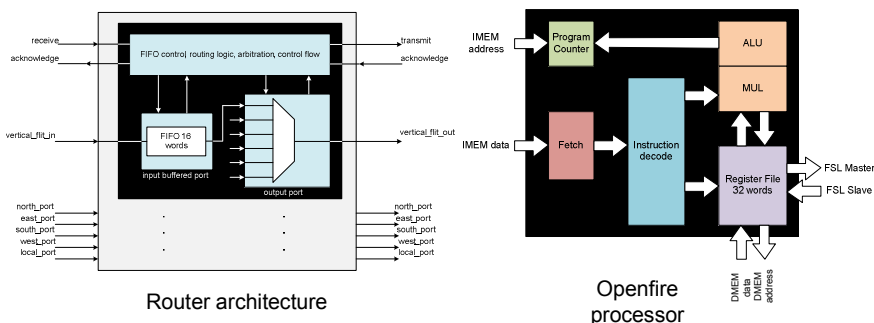
## 3D Technology



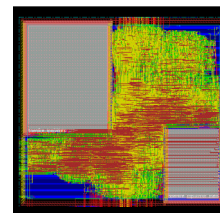
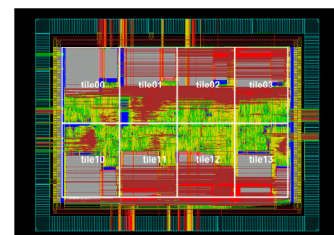
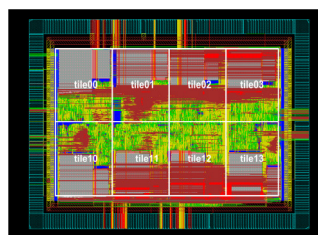
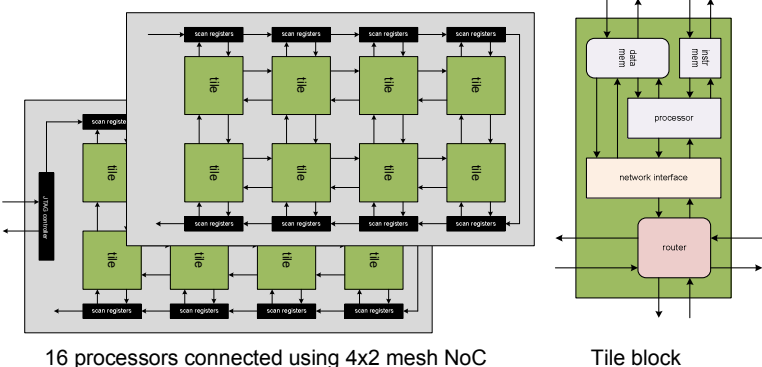
Two tier 3D stacking

## 3D Architecture

- Target operational frequency = 147 MHz (7 ns clock), target test frequency = 10 mHz
- Fully synchronous, off-chip interface using JTAG IEEE 1149.1
- Die size = 5.0 mm x 3.5 mm



## Physical Implementation



## References

[1] CMP, <http://cmp.imag.fr>

[2] Tao Zhang et al, "A 3D SoC design for H.264 application with on-chip DRAM stacking," *3D Systems Integration Conference (3DIC), 2010 IEEE International*, pp.1-6, 16-18 Nov. 2010

[3] Healy, M.B. et al, "Design and analysis of 3D-MAPS: A many-core 3D processor with stacked memory," *Custom Integrated Circuits Conference (CICC), 2010 IEEE*, pp.1-4, 19-22 Sept. 2010

[4] Van der Plas et al, "Design issues and considerations for low-cost 3D TSV IC technology," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, pp.148-149, 7-11 Feb. 2010

[5] Loi, I. et al, "3D NoCs — Unifying inter & intra chip communication," *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, pp.3337-3340, May 30 2010-June 2 2010

[6] Mineo, C., "Inter-die signaling in three dimensional integrated circuits," *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, pp.655-658, 21-24 Sept. 2008